Lab 09

Flip-Flops and Counters

ECE 380-002

University of Alabama

Yichen Huang

Thomas Dillman

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**Introduction**

In this lab, we mainly focusing on the design two types of flip-flops: one is edge-triggered D flip-flop and another one is JK flip-flop. Two create two components through body diagram files and VHDL code. We also created a BDC counter in two ways those are through VHDL code and another one is use D flip-flop. Finally, we upload these circuits to the DE1 board to test the circuit.

**Procedure**

1. **Prelab**
2. Design A
3. BDF File

A screenshot of a computer

Description automatically generatedWe create a BDF file and implement a D flip-flop; after we compiled, we run the test through waveform file.

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1. VHDL File

We create D flip-flop through VHDL code. After we compile the file, we run the waveform file to test our design.

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1. Design B
2. BDF File

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Description automatically generatedWe create the JK flip-flop through BDF file. After we compile the file, we run the waveform file to test it.

1. VHDL File

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Description automatically generatedWe create the JK flip-flop through VHDL code and then we test the file through the waveform file.

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1. Design C
2. VHDL

In this design, we implement a BCD counter through VHDL code. In this design, we have three input: Enable, Reset and CLK and 4-bits output Q.

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1. BCD Counter with LED display

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Description automatically generatedIn this design we create a BEF file and implement the symbols from previous design and lab2 design. We then design a code converter from lab8.

1. **During the lab**
   1. Design A
      1. Part I

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Description automatically generatedIn this part we assign the input and output to the pin planner then we compiled again. Finally, we upload the design to the board, and we do the test on the board.

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* + 1. Part II

In this part we repeat the same procedure in the previous part.

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* 1. Design B
     1. Part I

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Description automatically generatedIn this part, we assign input and output of JK flip-flop to the pin. Then we compiled the file again. Finally, we upload the design to the upload to DE1 board and run the test.

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* + 1. Part II

We do the same procedure in the previous part.

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* 1. Design C

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Description automatically generatedFor the design C, we assigned the input and output then compiled the file again. After we upload the design to the board, we start test.

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**Result**

All the designs are tested. The result is same as we expected.

**Conclusion**

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